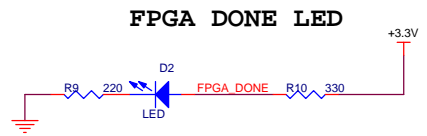
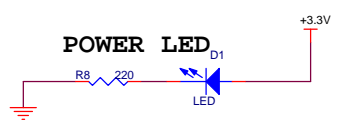
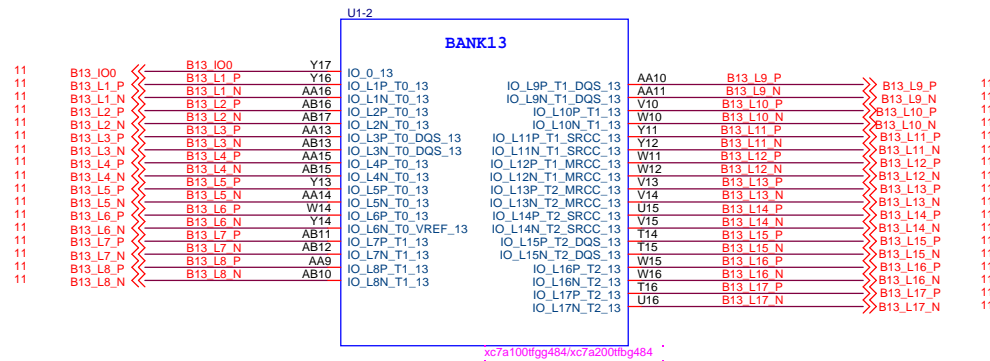
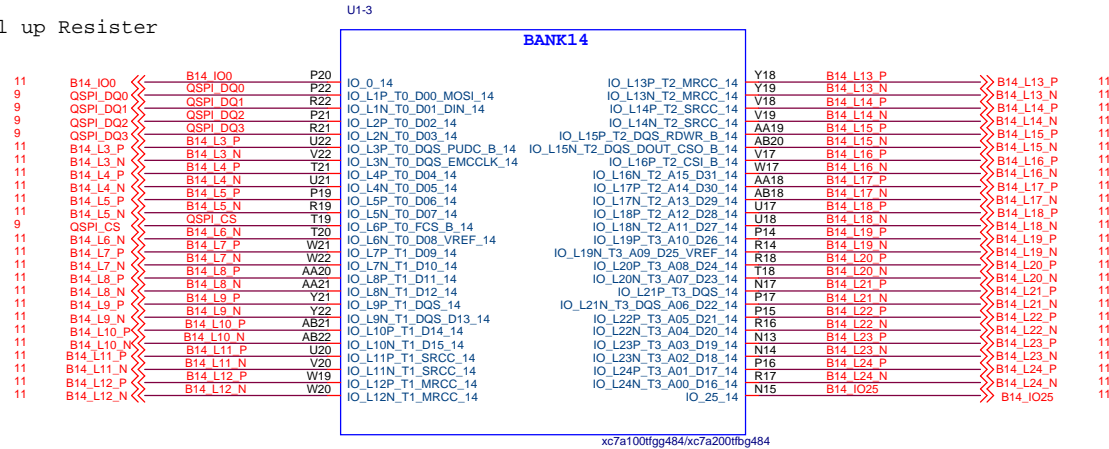
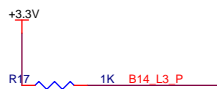


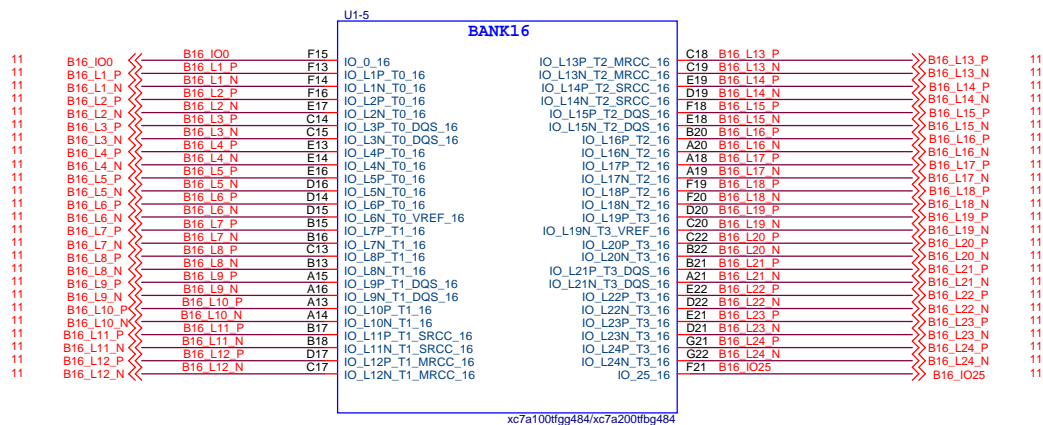
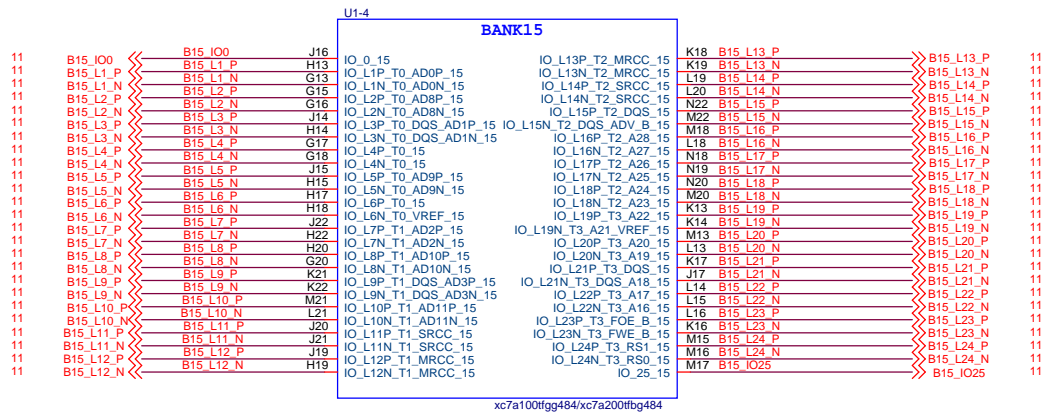
MASTER SPI x4
M[2:0] = 001



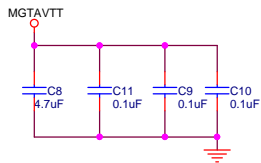


PUDC_B=1: Deactive internal Pull up Resister

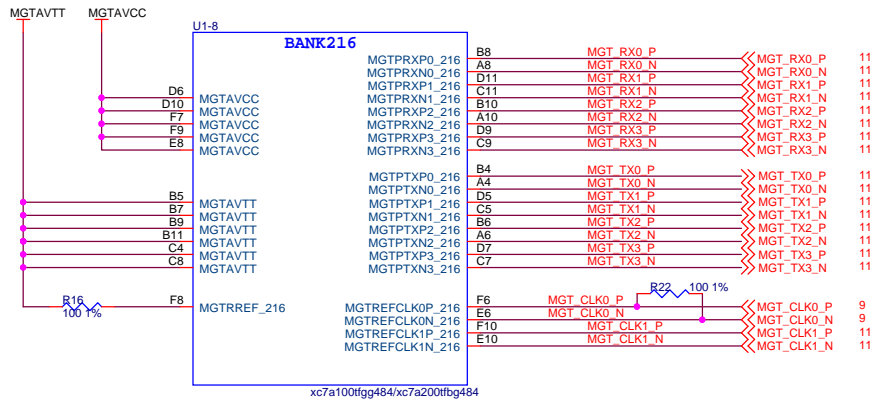
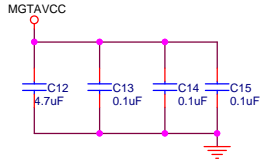


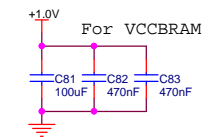
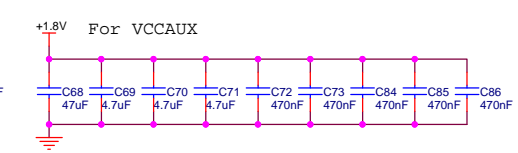
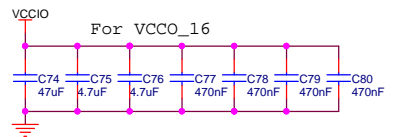
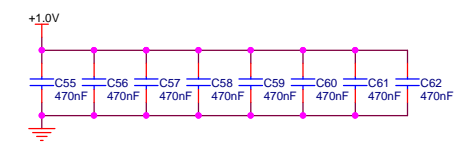
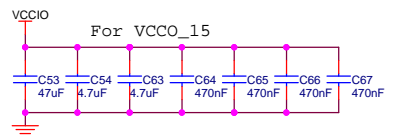
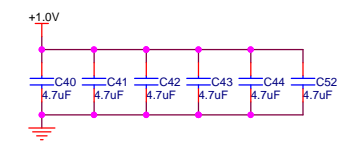
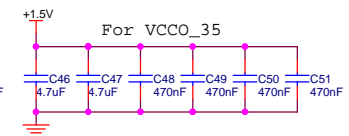
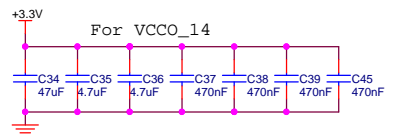
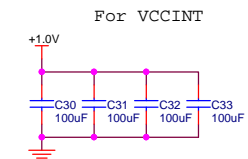
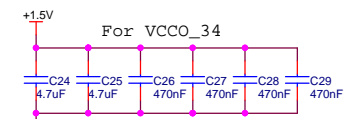
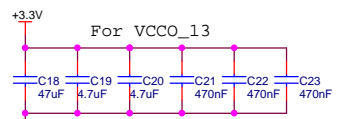
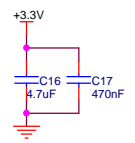
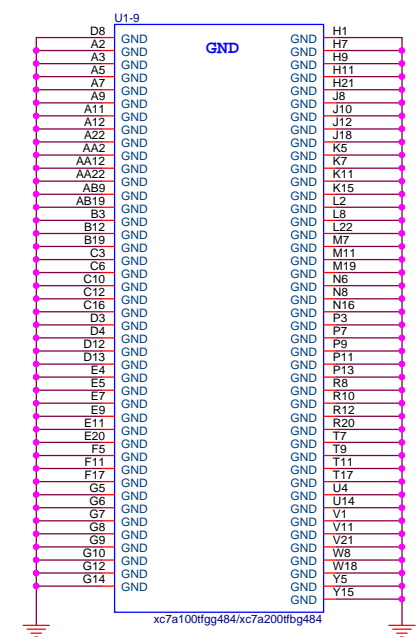
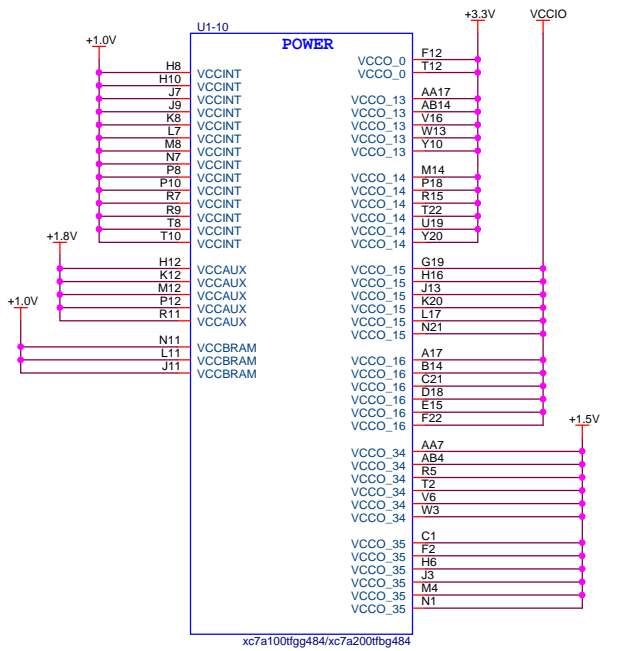


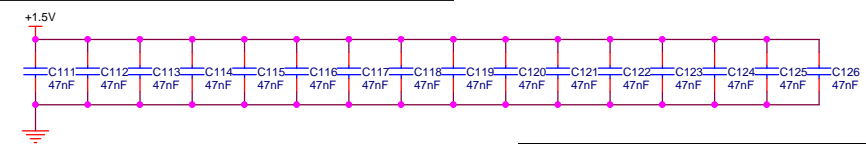
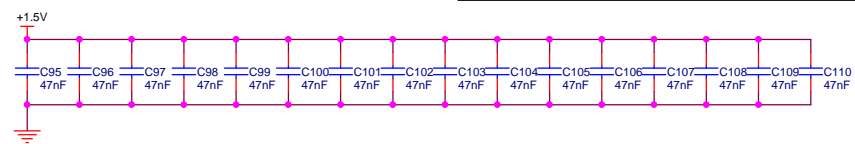
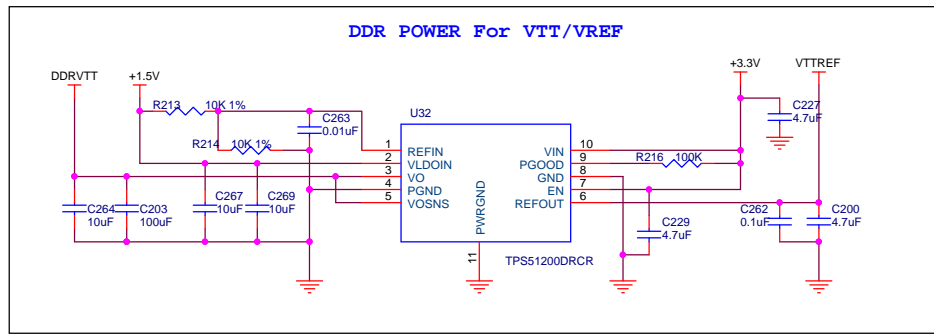
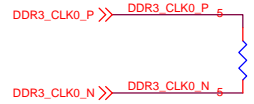
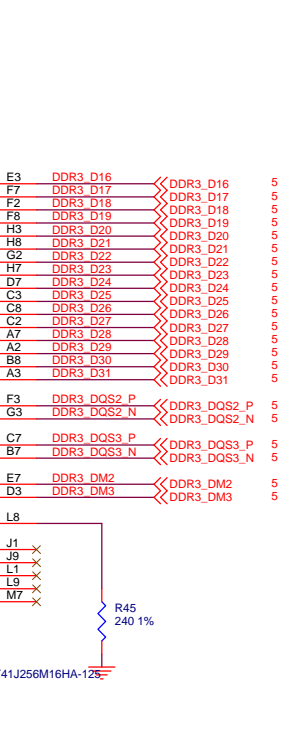
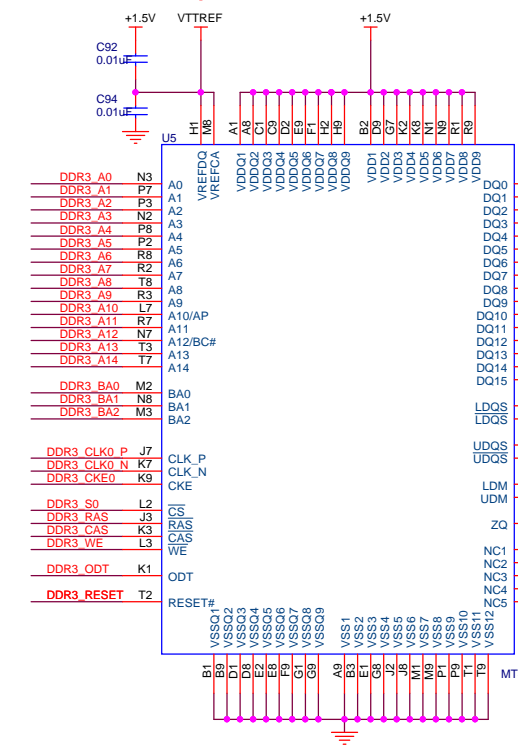
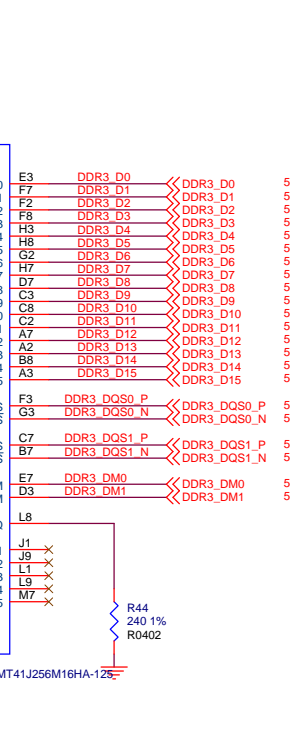
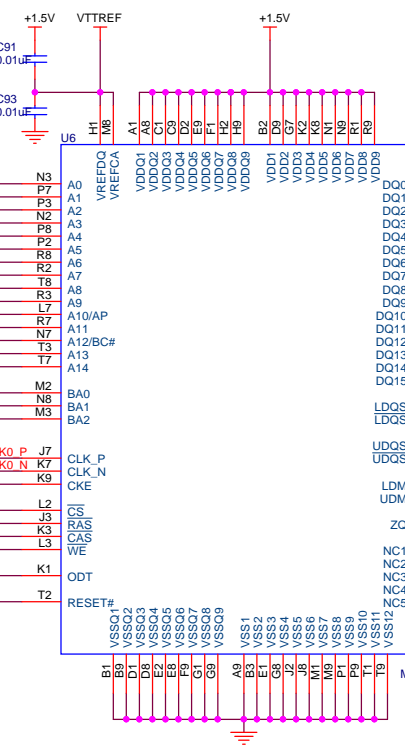
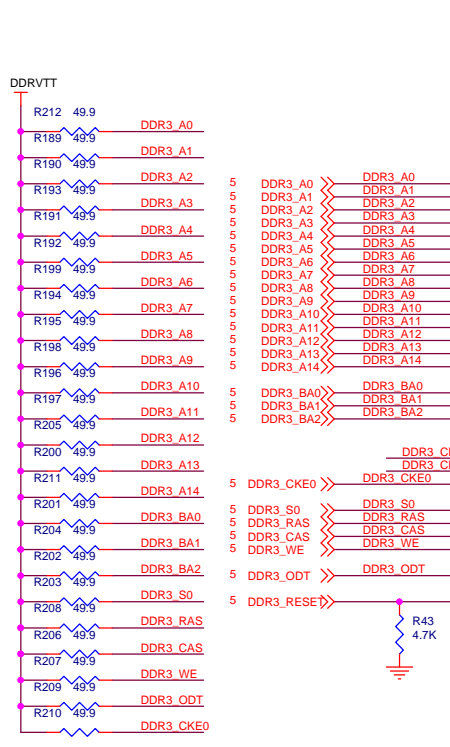
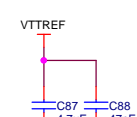
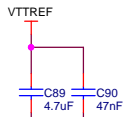
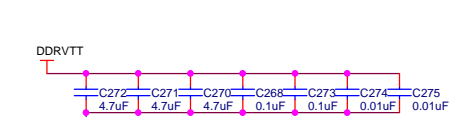
MGTAVTT 4.7uF(1) 0.1uF(2)



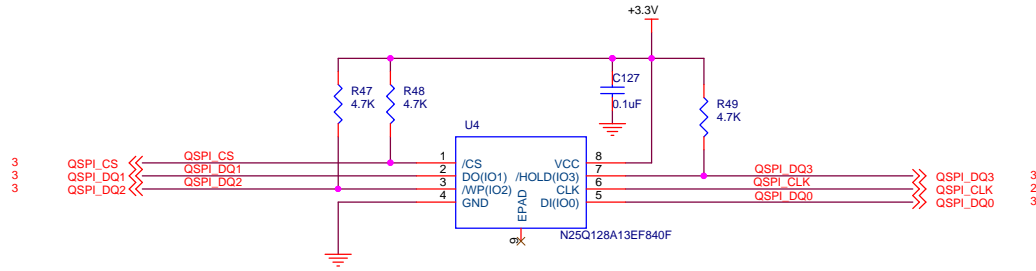
MGTAVCC 4.7uF(1) 0.1uF(2)





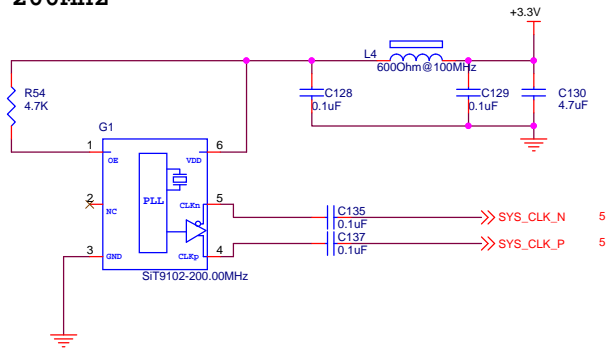


FPGA CONFIG SPI



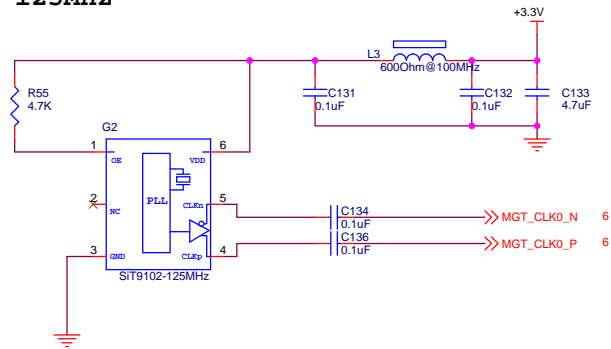
SYSTEM CLOCK

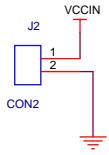
200MHz



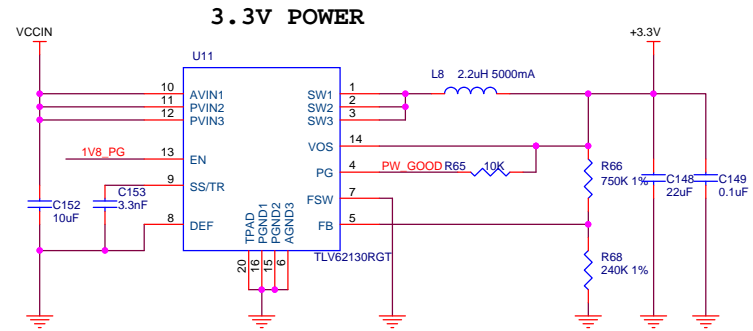
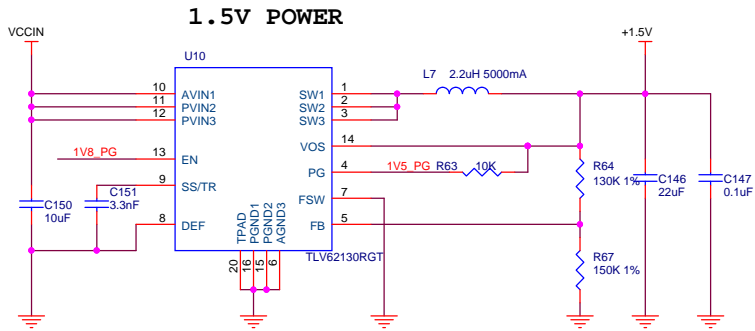
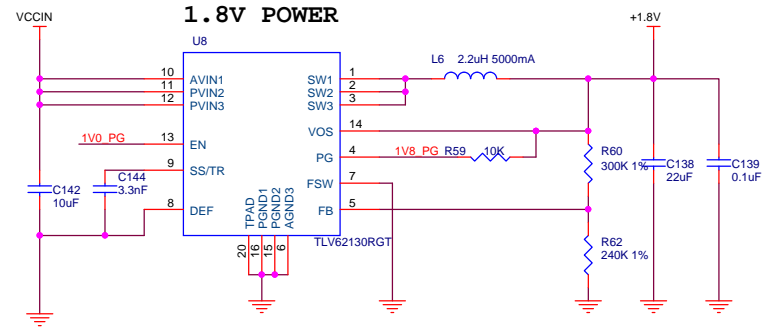
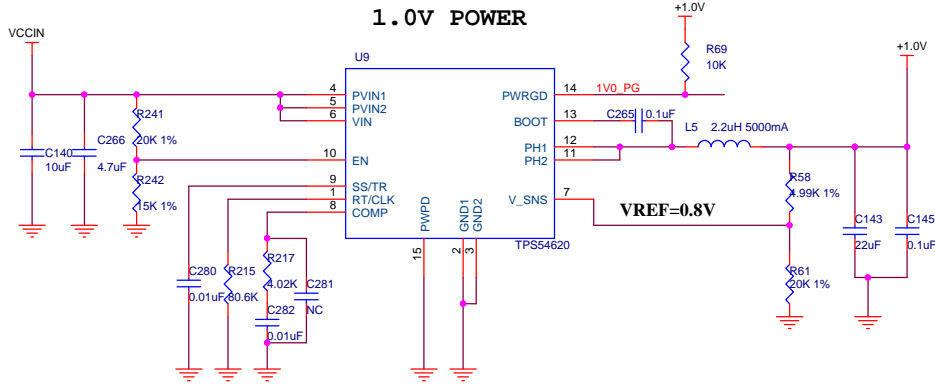
GTP CLOCK

125MHz





POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)



POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)

